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TITLE: Simultaneous read and refresh of different rows in a dram

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A memory array configuration of memory cells that allows simultaneous read and refresh of the memory cells includes M rows and N columns of memory cells, each row being arranged into a top half-row of N/2 memory cells corresponding to each odd-numbered column and a bottom half-row of N/2 memory cells corresponding to each even-numbered column. Each memory cell in the top half-row has a write column node coupled to a respective write column line, a read column node coupled to a respective read column line, a write row node coupled to a respective first write row line, and a read row node coupled to a respective read row line. Each memory cell in the bottom half-row has a write column node coupled to a respective write column line, a read column node coupled to a respective read column line, a write row node coupled to a

respective second write row line, and a read row node coupled to a respective read row line. A row of N/2 charge sensing **amplifiers** each has a first input coupled to an odd-numbered write column line and a second input coupled to a next even-numbered write column. A row of N current/voltage sensing **amplifiers** each has an input coupled to one of the read column lines and an output for providing a digital signal.

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A functional block diagram of a typical DRAM, the MT4C4003 1 megabit.times.4 DRAM manufactured by Micron Technology, Inc. of Boise, Id., is shown in FIG. 1. The DRAM memory contains approximately 4 megabits organized into four 1 megabit memory arrays 10A-10D. Circuit block 50 includes sense **amplifiers** coupled to each column within the memory array to transform charge on the capacitor in the memory cell into a valid logic one or zero. During read and write cycles, each bit in one of the four memory arrays is uniquely addressed through twenty address bits that are entered ten bits (A0-A9) at a time. The RAS signal (row address strobe) latches the first ten bits and the CAS signal (column address strobe) latches the latter ten bits. A read or write cycle is initiated with the WE signal (write

enable). The four data inputs/outputs (DQ1-DQ4) are routed through four pins using a common input/output bus controlled by the WE signal and an OE signal (output enable).

According to the present invention, a memory array configuration of memory cells that allows simultaneous read and refresh of the memory cells includes M rows and N columns of memory cells arranged in a folded architecture. Each row is arranged into a top half-row of N/2 memory cells corresponding to each odd-numbered column and a bottom half-row of N/2 memory cells corresponding to each even-numbered column. Each memory cell in the top half-row has a write column node coupled to a respective write column line, a read column node coupled to a respective read column line, a write row node coupled to a respective first write row line, and a read row node coupled to a respective read row line. Each memory cell in the bottom half-row has a write column node coupled to a respective write column line, a read column node coupled to a respective read column line, a write row node coupled to a respective second write row line, and a read row node coupled to a respective read row line. A row of N/2 charge sensing **amplifiers** each has a first input coupled to an odd-numbered write column line and a second input coupled to a next

even-numbered write column. A row of N current/voltage sensing **amplifiers** each has an input coupled to one of the read column lines and an output for providing a digital signal.

In operation, one of the entire rows of memory cells is read-selected, which transfers charge in the memory cells to the respective read column node and read column line. The current/voltage sensing **amplifiers** respectively coupled to the read column node of each of the memory cells transforms the charge into a valid logic signal to complete a normal read operation. Simultaneously during the read operation, each of the write column lines is normalized to a reference level that is halfway between the logic one and zero charge levels. A second half-row of memory cells is write-selected, which transfers charge in the memory cells to the respective write column node and write column line. In the present memory array configuration, a pair of write column lines contains a charge from the memory cell, and the other write column line in the pair retains the reference level. Therefore, the charge **amplifiers** force complementary valid logic levels on each successive pair of write column lines responsive to the charge difference in the write column lines to simultaneously refresh the second half-row while the first

half-row is being read. The first and second half-rows are entirely separate and need not be adjacent in the array.

FIG. 4 is a schematic diagram of a prior art charge sensing **amplifier** suitable for use in the present invention; and

FIG. 5 is a schematic diagram of a prior art current/voltage sensing **amplifier** suitable for use in the present invention.

Referring now to FIG. 3, the first four columns C1-C4 of the array 10 are depicted and the first two rows of the array are depicted. Each half-row is labeled. For example, the first row is labeled R1A and R1B designating the top and bottom half-rows. A row of N/2 charge sensing **amplifiers** 22 has a first input coupled to an odd-numbered write column line and a second input coupled to a next even-numbered write column. A row of N current/voltage sensing **amplifiers** 24 in circuit block 50 has an input coupled to one of the read column lines and an output 28 for transforming the charge on the read column line into a valid digital signal. The row of N current/voltage sensing **amplifiers** 24 sense the voltage drop across (or the current flow through) a row

of N P-channel pull-up transistors 26.

Referring now to FIG. 4, a charge sensing **amplifier** 22 suitable for use in the present invention includes a differential strobe input for selectively enabling and disabling charge amplification. Taking the STROBE signal to a logic one enables the amplification of the charge sensing **amplifier** 22. **Amplifier** 22 includes first and second P-channel transistors 42 and 43. The sources of transistors 42 and 43 are coupled together and to the positive supply voltage, VCC, typically equal to five volts, through the P-channel strobe transistor 41. The P-channel strobe transistor 41 is energized with an inverted STROBE signal. **Amplifier** 22 further includes third and fourth N-channel transistors 44 and 45. The sources of transistors 44 and 45 are coupled together and to a negative supply voltage or ground (GND), through the N-channel strobe transistor 46. The N-channel strobe transistor 46 is energized with a non-inverted STROBE signal. The drains of the first and third transistors 42 and 44 and the gates of the second and fourth transistors 43 and 45 are coupled together to form the first input, WC1. The drains of the second and fourth transistors 43 and 45 and the gates of the first and third

transistors 42 and 44 are coupled together to form the second input, WC2.

In operation, small changes in charge on the word column lines establish a small positive or negative voltage differential across the inputs to the charge sensing **amplifier** 22. The small change is amplified by the positive feedback configuration of the **amplifier**, which ultimately establishes a full, valid logic level at the inputs. A logic one appears at the input that was originally slightly more positive than the other input, and, conversely, a logic zero appears at the input that was originally slightly more negative than the other input.

Referring now to FIG. 5, a current/voltage sensing **amplifier** 24 suitable for use in the present invention includes a differential load formed by P-channel transistors 31 and 32. The gate and drain of transistor 31 are coupled together to form a first node and the drain of transistor 32 forms a second nodes. First and second N-channel transistors 33 and 34 form a differential voltage **amplifier** wherein the sources are coupled together and receive a bias current provided by N-channel transistor 35. The drains of the first and

second transistors 33 and 34 are respectively coupled to the first and second nodes of the differential load 31, 32 to provide gain for the **amplifier** 24. The gate of the first transistor 33 forms the input, RC, the drain of the second transistor 34 forms the output 28, and the gate of the second transistor 34 is coupled to a reference voltage source, VREF, which can be between VCC-VT and VCC/2. The gates of transistors 33 and 34 are interchangeable, but the polarity of the output 28 is then inverted.

Referring back to FIG. 3, a read operation is conventionally performed by read-selecting an entire row and reading data out at the output 28 of the voltage sensing **amplifiers** 24. Read-selection of one of the entire row of memory cells is typically accomplished by coupling the read row line RR of the entire row to a logic low to couple charge from the memory cell 20 to the respective read column line RC. The respective write row lines WRA or WRB are coupled to a logic low to prevent new data from being read into the memory cells and corrupting the data during the read operation. The polarity of the read and write row lines is typically taken low for enabling the reading of data and preventing the writing of data. However, these polarities may be

different in some types of dual-port memory cells.

Simultaneously, during the reading operation of the first half-row of memory cells, another half-row is write-selected in order to refresh the data in the memory cells. During a read operation, each of the write column lines is normalized to a reference level, usually VCC/2, or 2.5 volts. A second half-row of memory cells is write-selected in order to share stored charge in the memory cell with a corresponding write column line. Write-selection of one of the half-rows of memory cells is typically accomplished by coupling the write row line WRA or WRB to a logic high. Thus, a small incremental voltage is produced on a pair of write column lines. One of the pair of write column lines remains at the reference level, while the other of the pair is slightly more negative or positive depending upon the polarity of the data in the memory cell 20. The charge sensing **amplifiers** 22 coupled between the pair of write column lines force complementary valid logic levels on successive pairs of write column lines responsive to the charge difference in the write column lines. The charge sensing **amplifiers** are enabled through the STROBE signal during the simultaneous read and refresh operation. Once a valid logic level

is established, this level restores the data in the memory cell through the write column node of the memory cell 20.

Although the present invention allows the user to read an entire row while selecting another half-row to refresh, it is apparent that the same row can be read and refreshed. As before, each of the write column lines are normalized to the reference level during the read operation. However, the current half-row of memory cells cannot be refreshed until the current/voltage sense **amplifiers** 24 settle. Therefore, the refresh cycle is delayed for a time to permit the current/voltage sense **amplifiers** to settle. After the current/voltage sensing **amplifiers** 24 have settled, the same half-row of memory cells is write-selected to share stored charge with the write column line. The charge sensing **amplifiers** 22 are enabled which forces complementary valid logic levels on the successive pairs of write column lines responsive to the charge difference in the write column lines. The same half-row is therefore refreshed after completing a read operation.

a row of N/2 charge sensing **amplifiers** having a first input coupled to an odd-numbered write column line and a second input coupled to a next even-numbered write column; and

a row of N current/voltage sensing **amplifiers** having an input coupled to one of the read column lines and an output for providing a digital signal.

4. A memory array configuration as in claim 2 in which at least one of the charge sensing **amplifier** comprises means coupled to a strobe input for selectively enabling and disabling the amplification of the charge sensing **amplifier**.

5. A memory array configuration as in claim 2 in which at least one of the charge sensing **amplifiers** comprises:

7. A memory array configuration as in claim 2 in which at least one of the current/voltage **amplifiers** comprises:

providing a row of N/2 charge sensing **amplifiers** having first and second inputs;

coupling the first input of each of the charge sensing **amplifiers** to an odd-numbered write column line and the second input of each of the charge sensing **amplifiers** coupled to a next even-numbered write column;

providing a row of N current/voltage sensing **amplifiers** having an input and

an output;

coupling the input of each of the current/voltage sensing **amplifiers** to one of the read column lines;

providing a digital signal at the output of each of the current/voltage sensing **amplifiers**;

reading data out at the output of the current/voltage sensing **amplifiers** respectively coupled to a read column node of each of the memory cells;

12. A method for allowing simultaneous reading and refresh of memory cells in a memory as in claim 9 in which the step of forcing complementary valid logic levels on successive pairs of write column lines comprises the step of enabling amplification in the charge sensing **amplifiers** with a strobe signal.